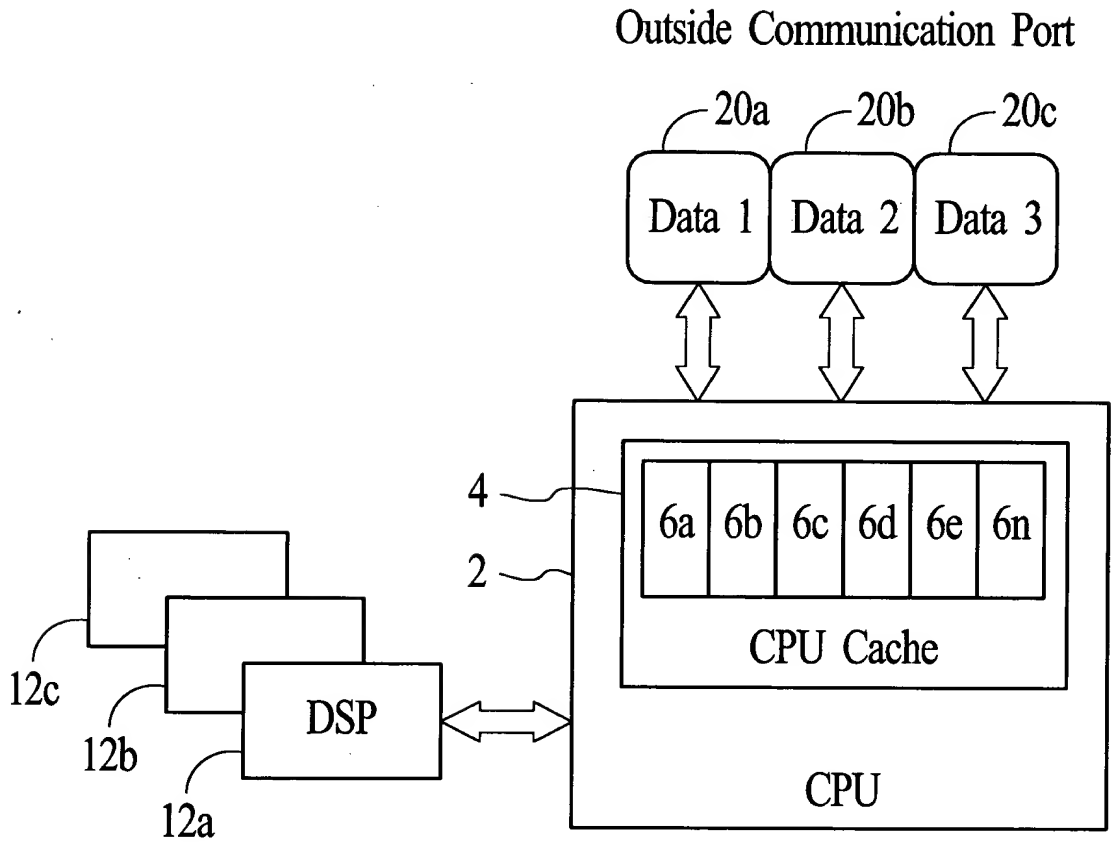


FIG. 1
(PRIOR ART)

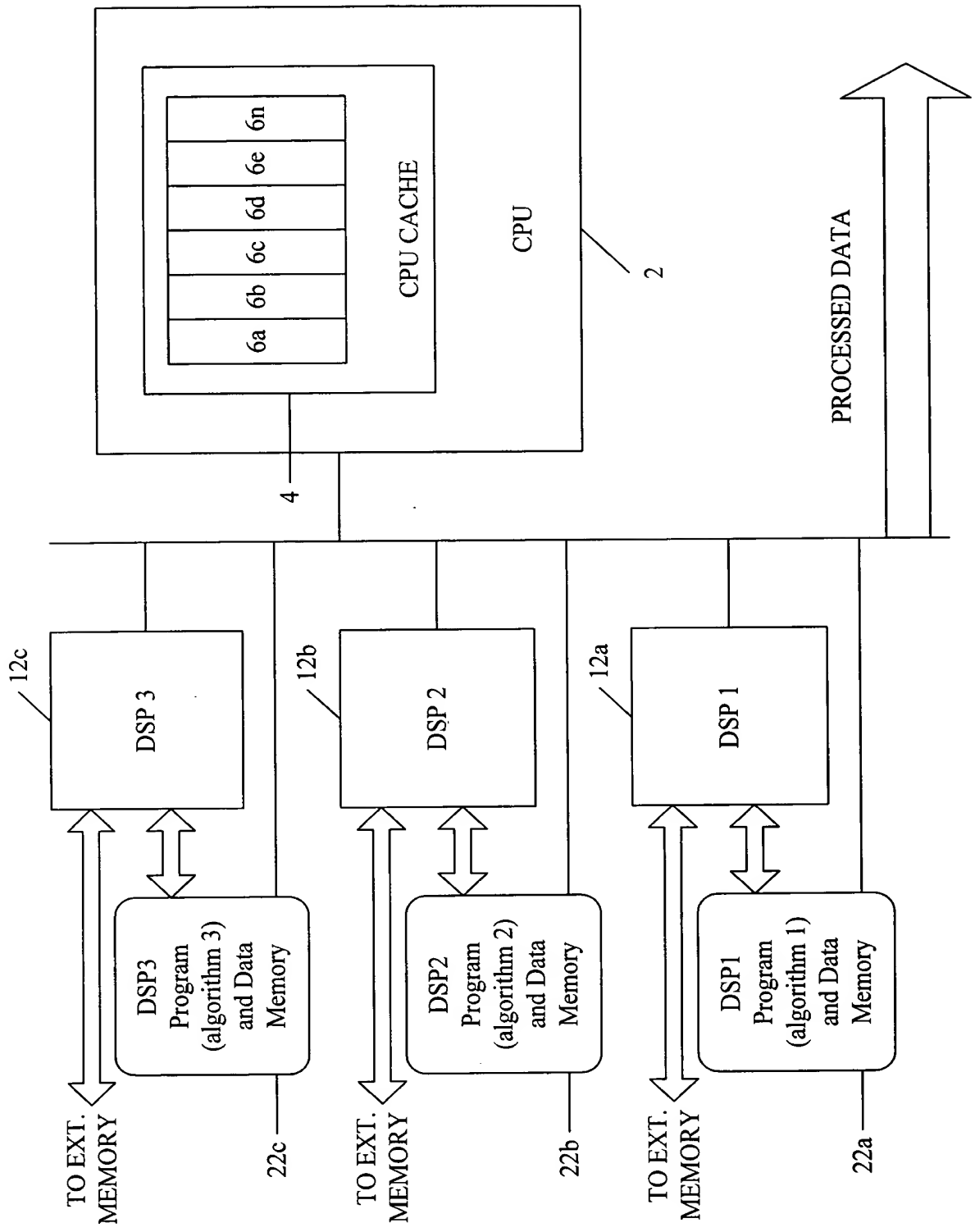


FIG. 2 (PRIOR ART)

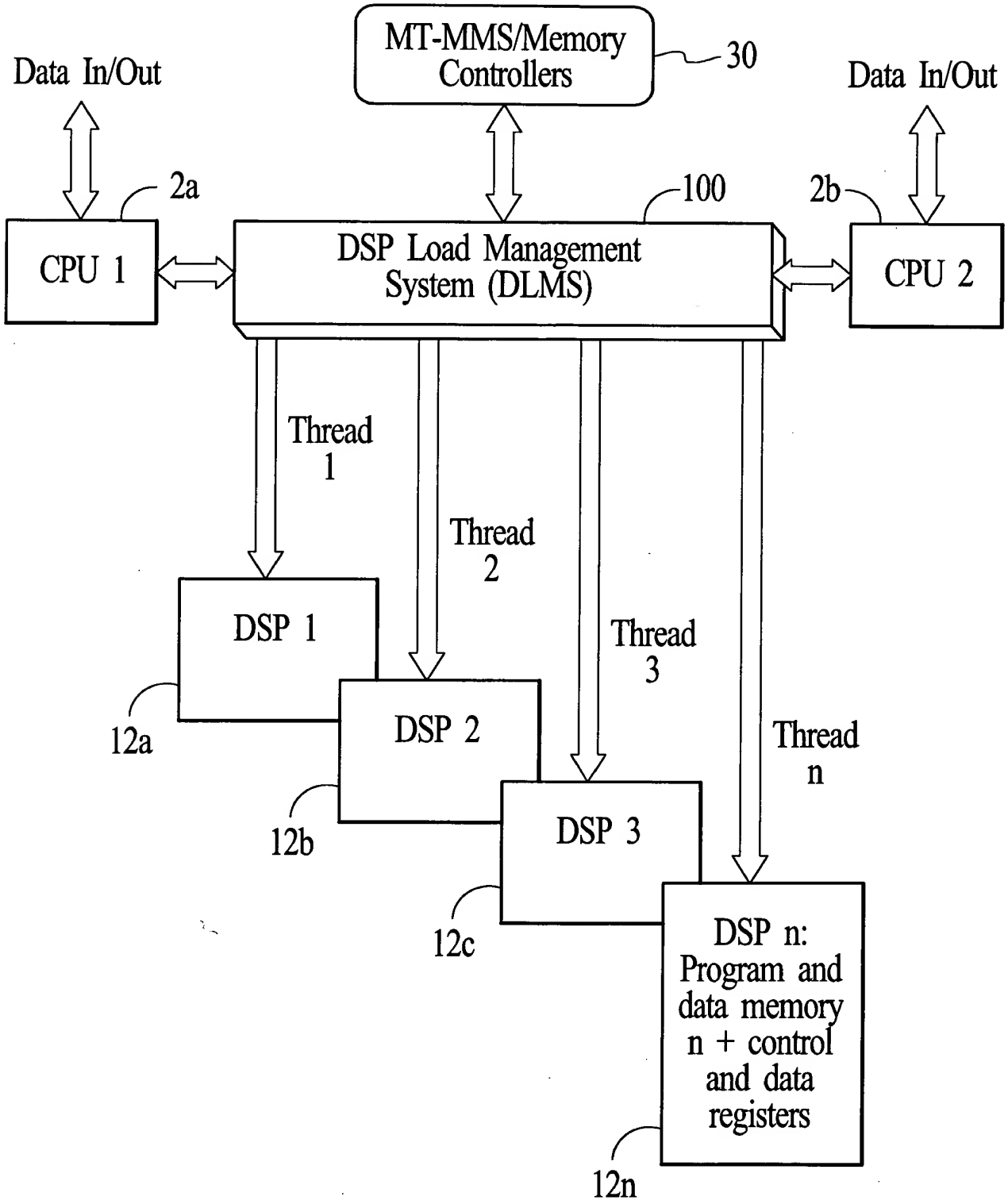

MT-MMS/Memory Controllers
30
Data In/Out
Data In/Out
2a
100
2b
CPU 1
DSP Load Management System (DLMS)
CPU 2
Thread 1
Thread 2
Thread 3
Thread n
DSP 1
DSP 2
DSP 3
DSP n: Program and data memory n + control and data registers
12a
12b
12c
12n

FIG. 3A

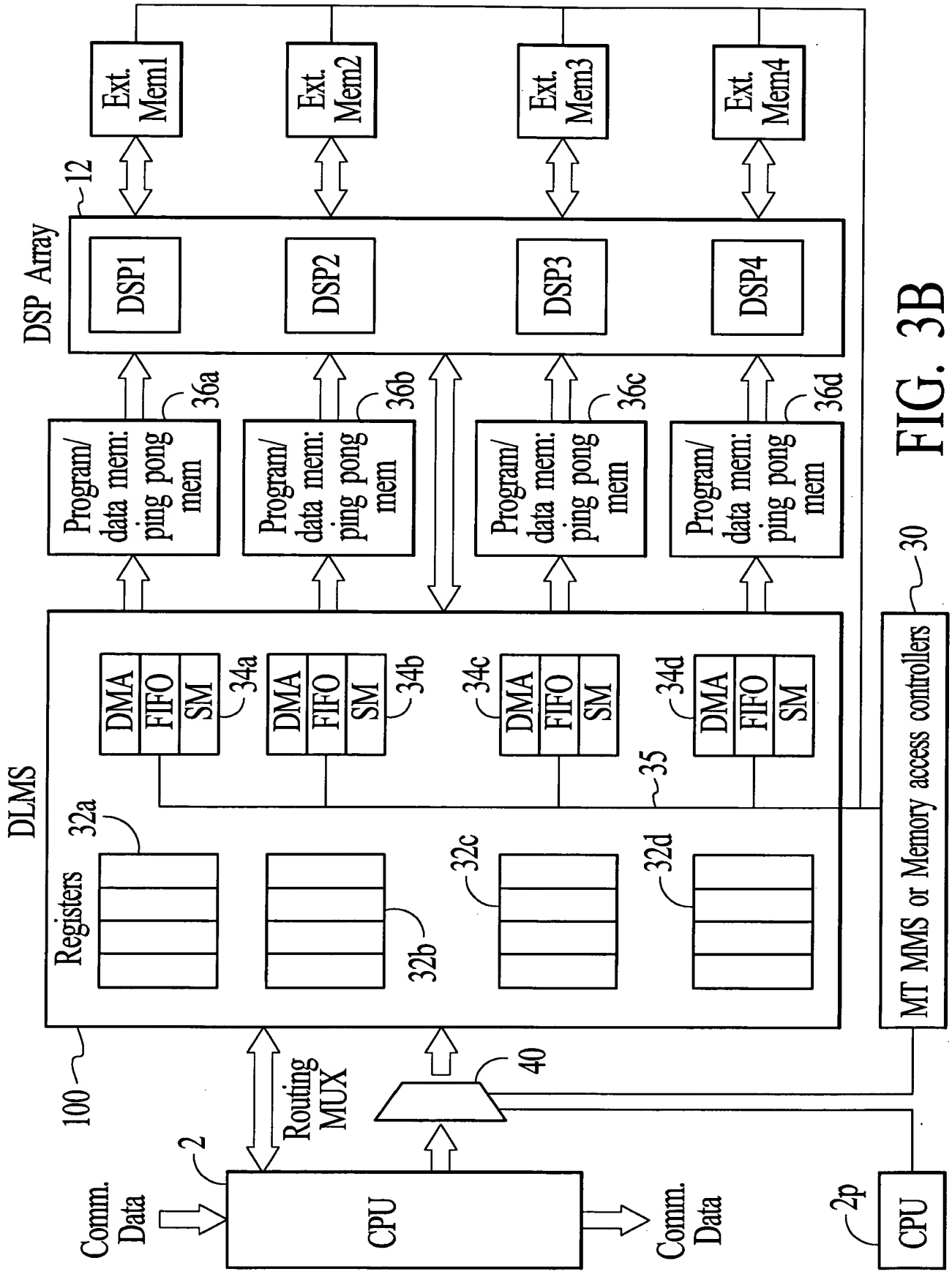

Ext. Mem1
Ext. Mem2
Ext. Mem3
Ext. Mem4
12
DSP Array
DSP1
DSP2
DSP3
DSP4
Program/ data mem: ping pong mem
36a
36b
36c
36d
DLMS
DMA
FIFO
SM
34a
34b
34c
34d
35
Registers
32a
32b
32c
32d
30
MT MMS or Memory access controllers
100
Routing MUX
40
2
Comm. Data
CPU
Comm. Data
2p
CPU

FIG. 3B

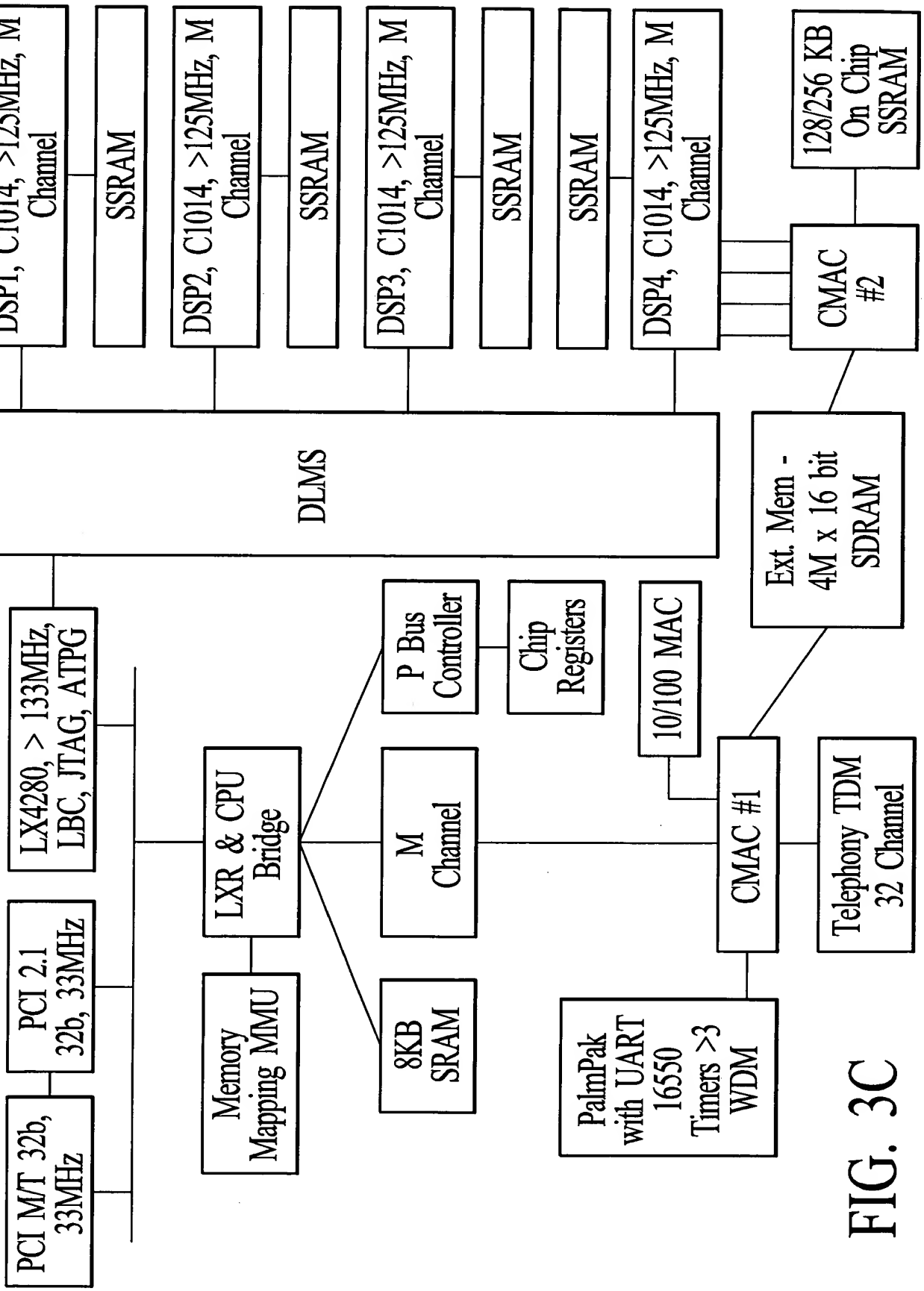

DSP1, C1014, >125MHz, M Channel
SSRAM
DSP2, C1014, >125MHz, M Channel
SSRAM
DSP3, C1014, >125MHz, M Channel
SSRAM
SSRAM
DSP4, C1014, >125MHz, M Channel
128/256 KB On Chip SSRAM
CMAC #2
DLMS
Ext. Mem - 4M x 16 bit SDRAM
LX4280, > 133MHz, LBC, JTAG, ATPG
P Bus Controller
Chip Registers
10/100 MAC
LXR & CPU Bridge
M Channel
CMAC #1
Telephony TDM 32 Channel
PCI 2.1 32b, 33MHz
PCI M/T 32b, 33MHz
Memory Mapping MMU
8KB SRAM
PalmPak with UART 16550 Timers >3 WDM

FIG. 3C

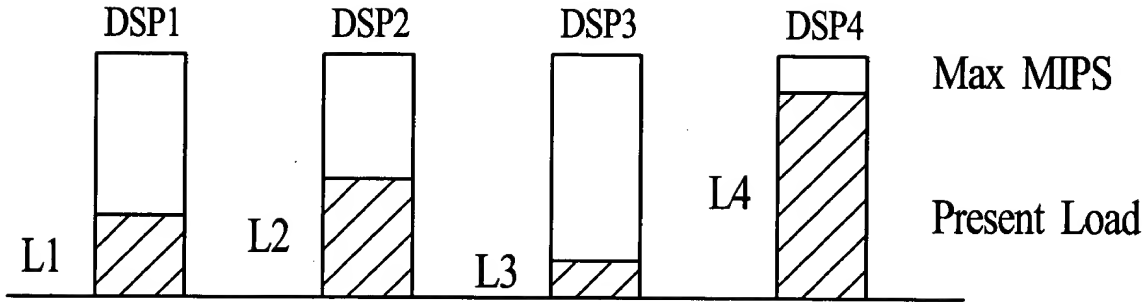


FIG. 4A

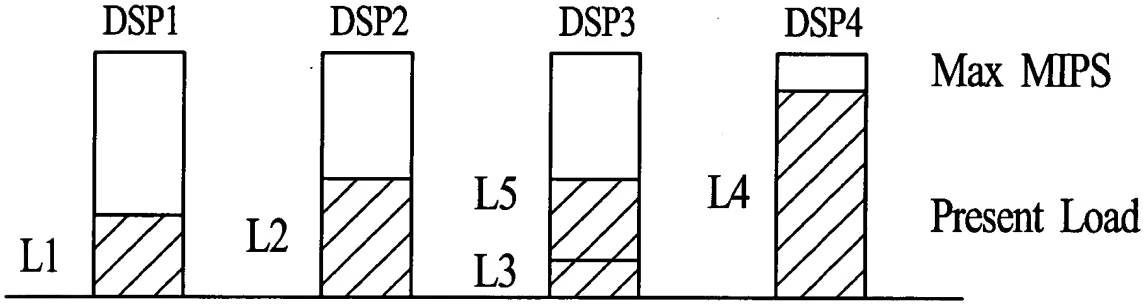


FIG. 4B

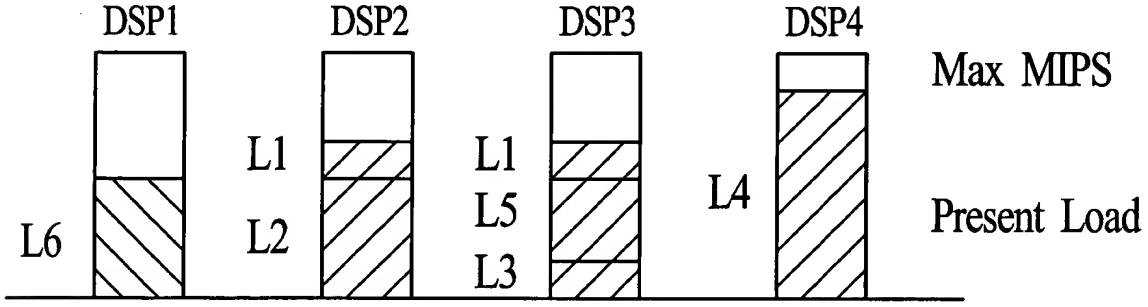


FIG. 4C

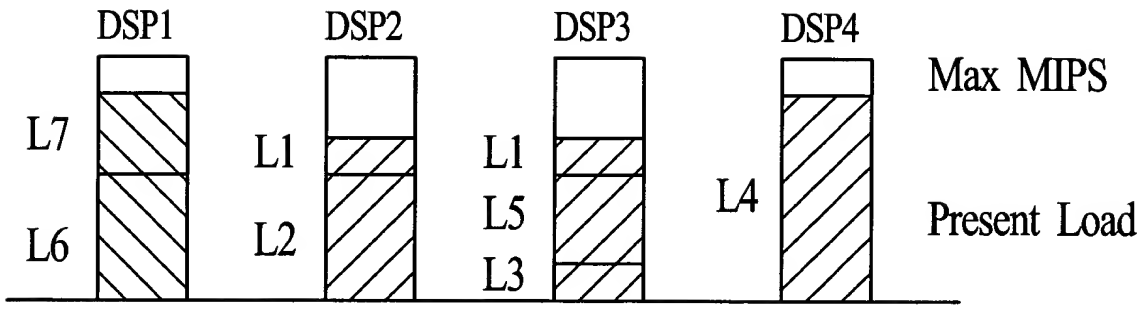


FIG. 4D

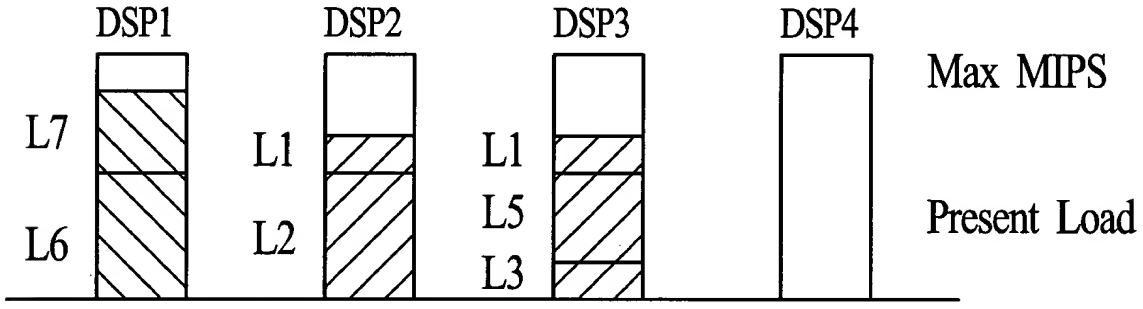


FIG. 4E

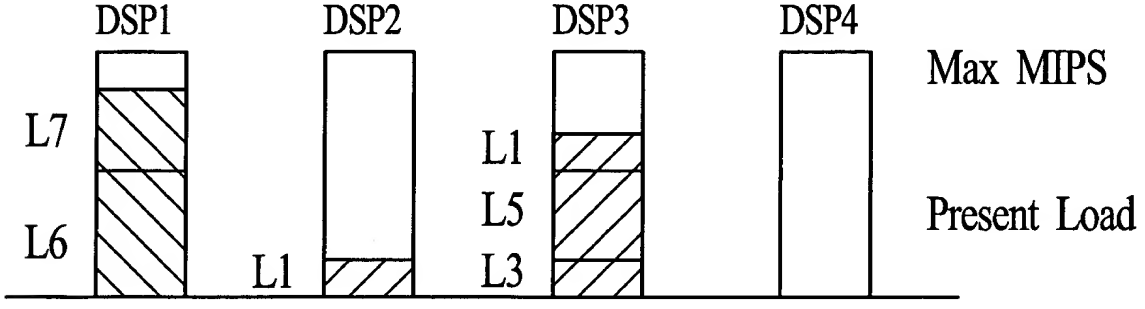


FIG. 4F

	DSP1	DSP2	DSP3	
Algorithm 1	15			
Algorithm 2		5		
Algorithm 3			2	
Algorithm 4			2	

FIG. 4G

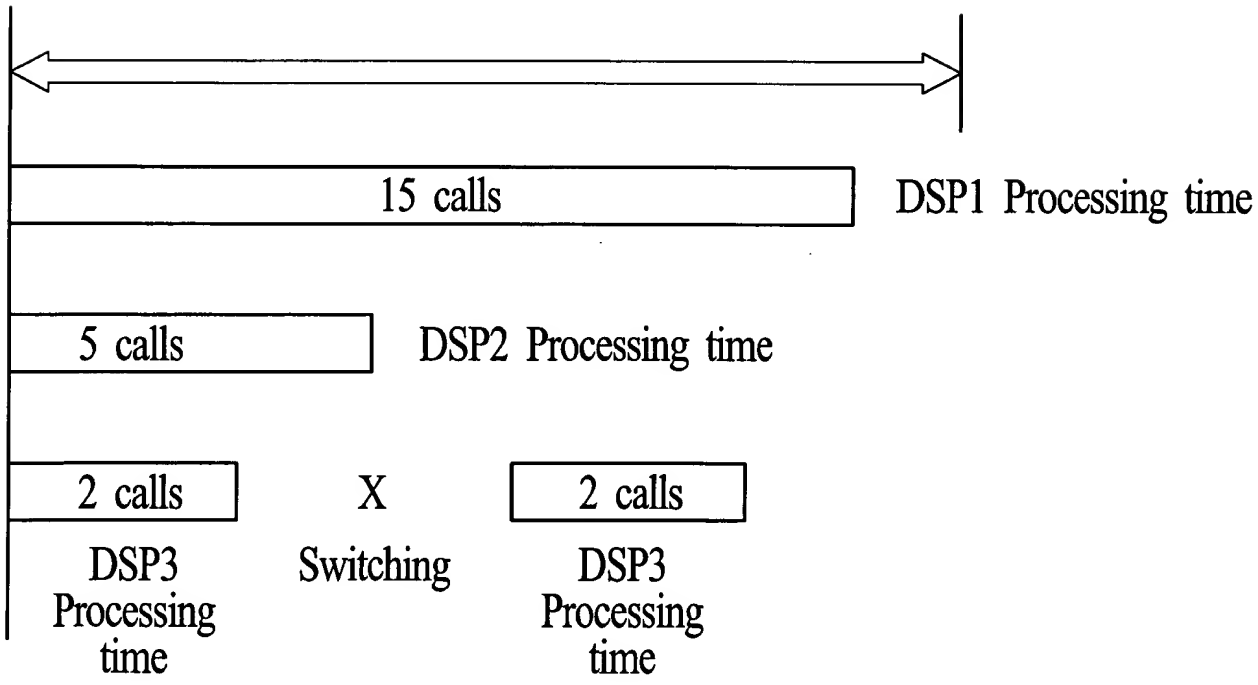


FIG. 4H

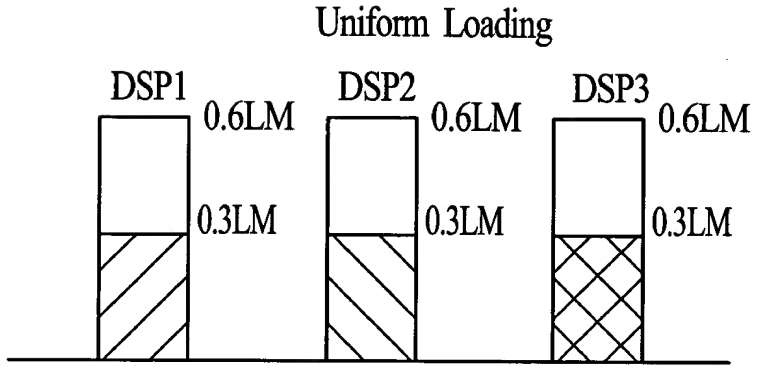


FIG. 5A

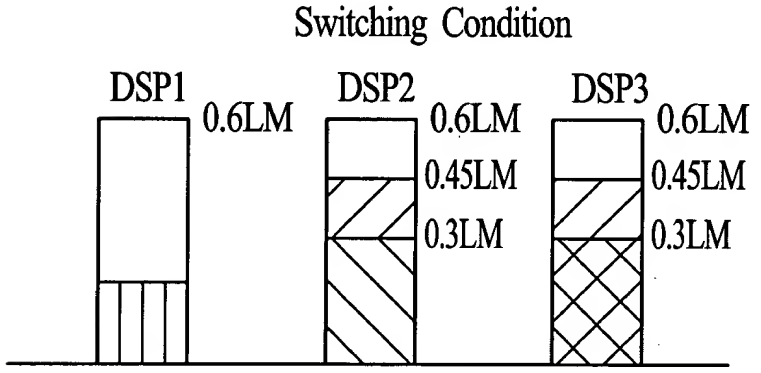


FIG. 5B

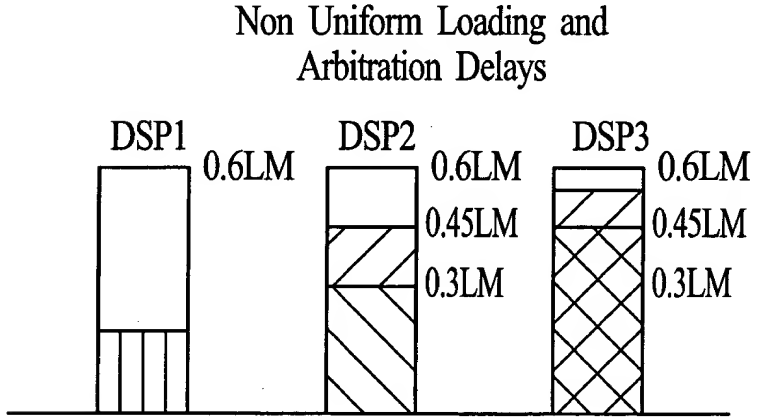


FIG. 5C

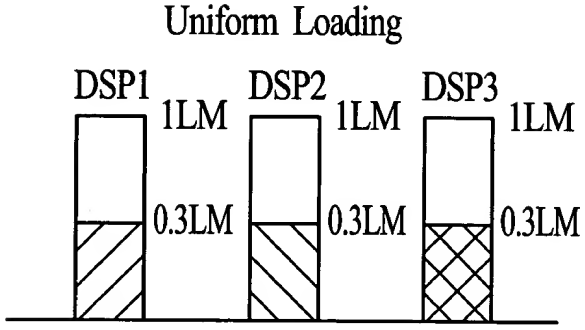


FIG. 6A

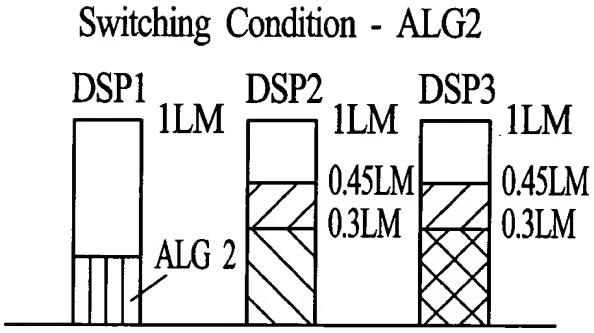


FIG. 6Bi

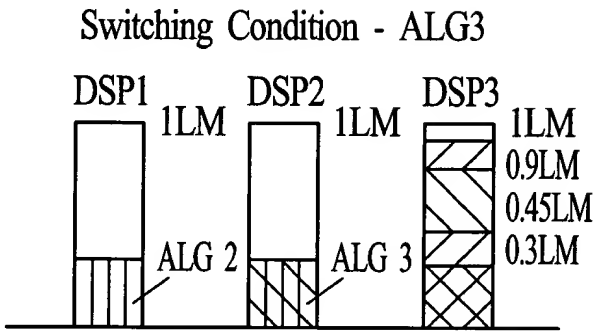


FIG. 6Bii

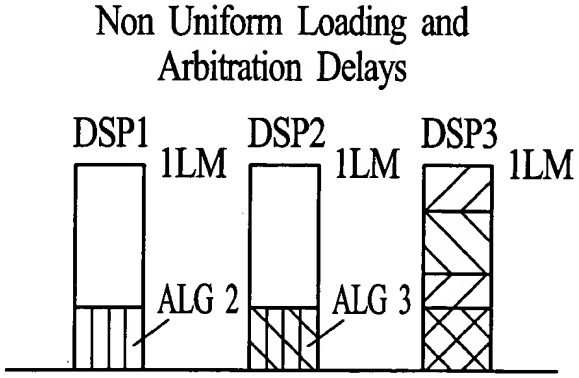


FIG. 6C

FIG. 7A

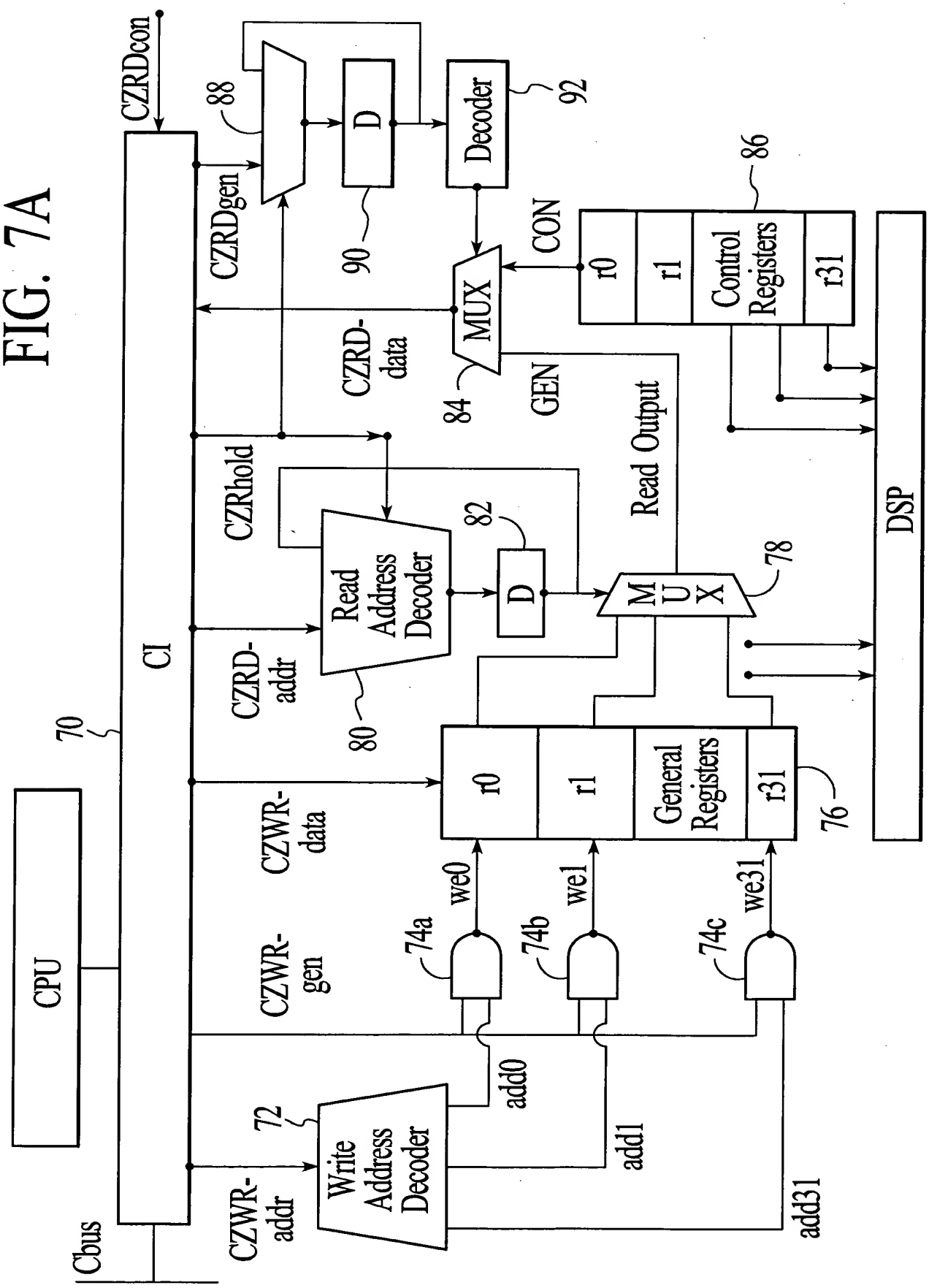
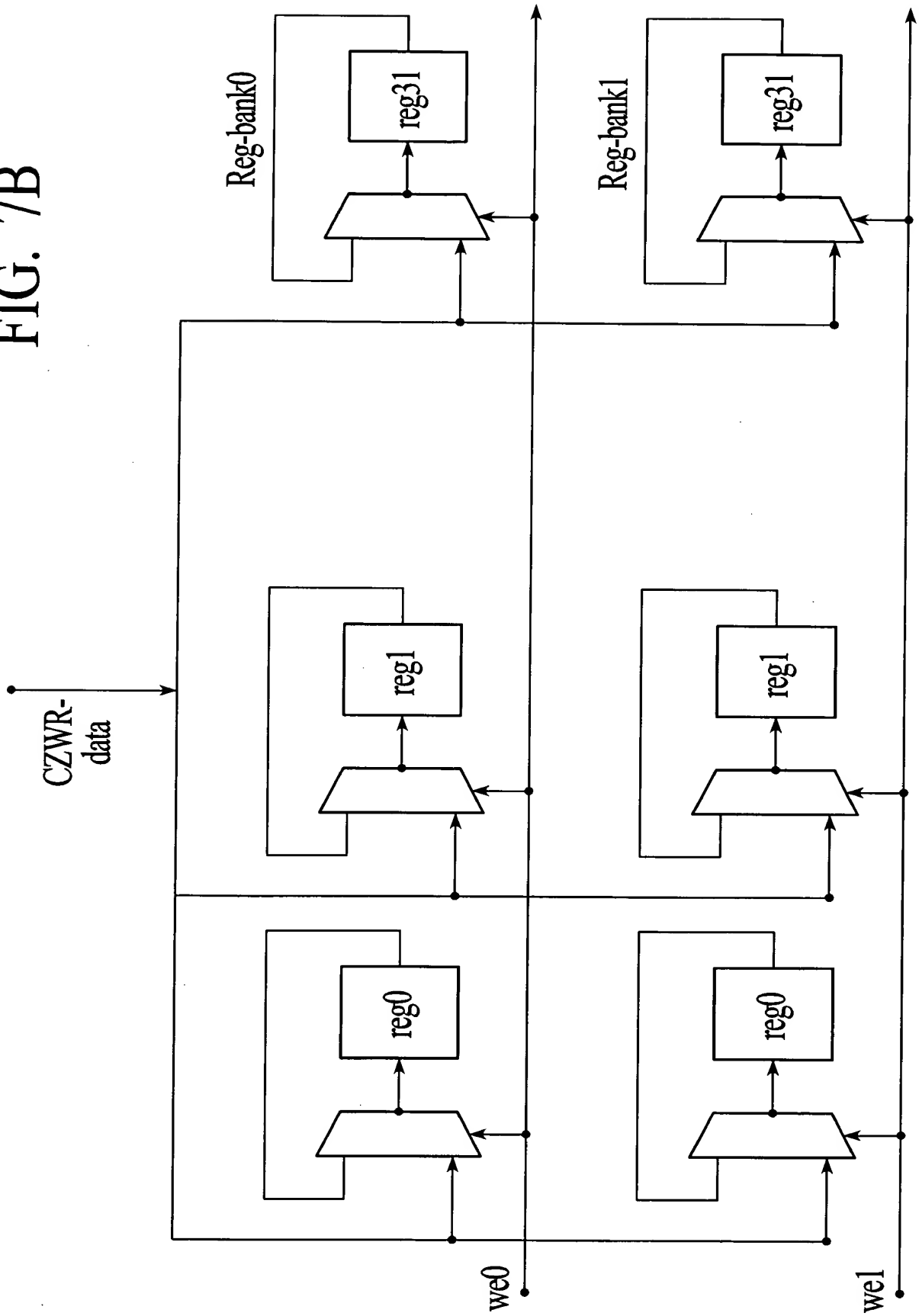

CZRDcon
88
D
Decoder
92
CZRDgen
90
CON
86
r0
r1
Control Registers
r31
MUX
CZRD-data
84
GEN
Read Output
DSP
CZRhold
82
Read Address Decoder
D
M U X
78
CZRD-addr
80
CI
70
CPU
r0
r1
General Registers
r31
76
CZWR-data
we0
we1
we31
CZWR-gen
74a
74b
74c
add0
add1
add31
72
Write Address Decoder
CZWR-addr
Cbus

FIG. 7B



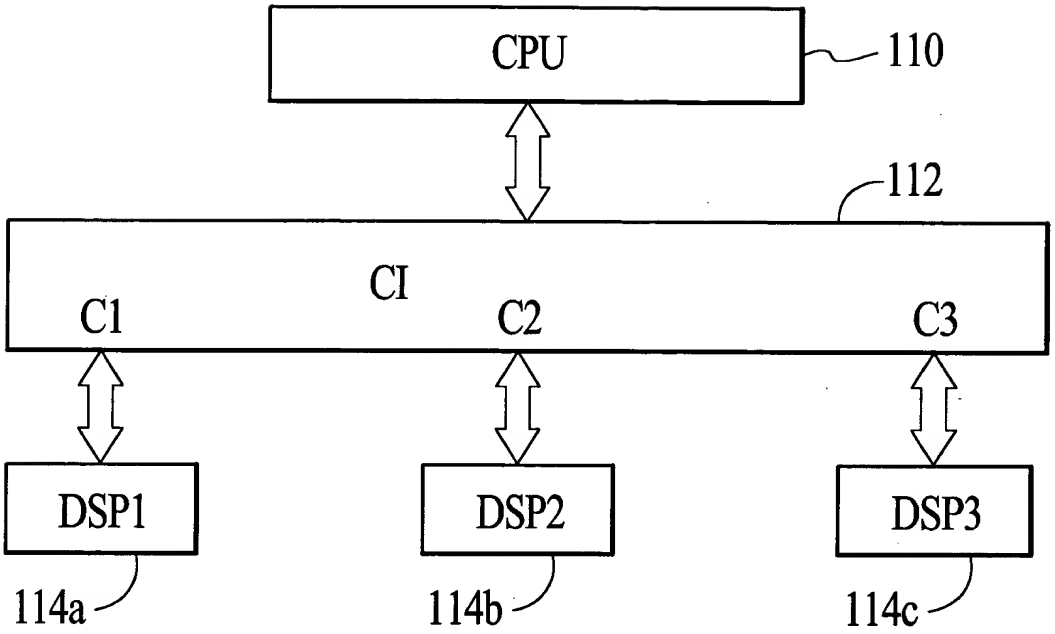

CPU
110
112
CI
C1
C2
C3
DSP1
DSP2
DSP3
114a
114b
114c

FIG. 8A

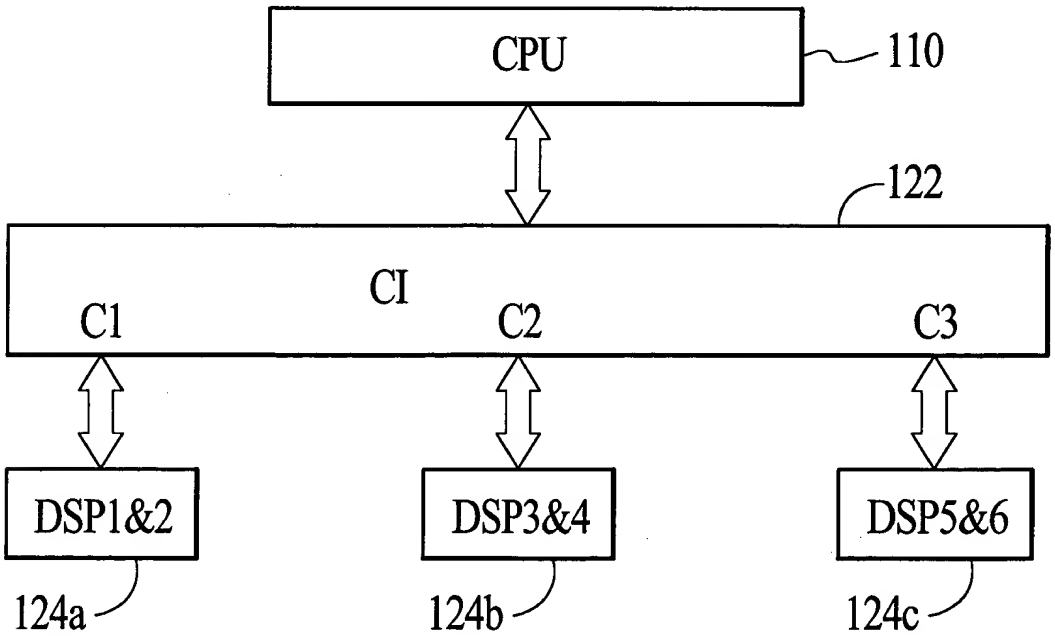
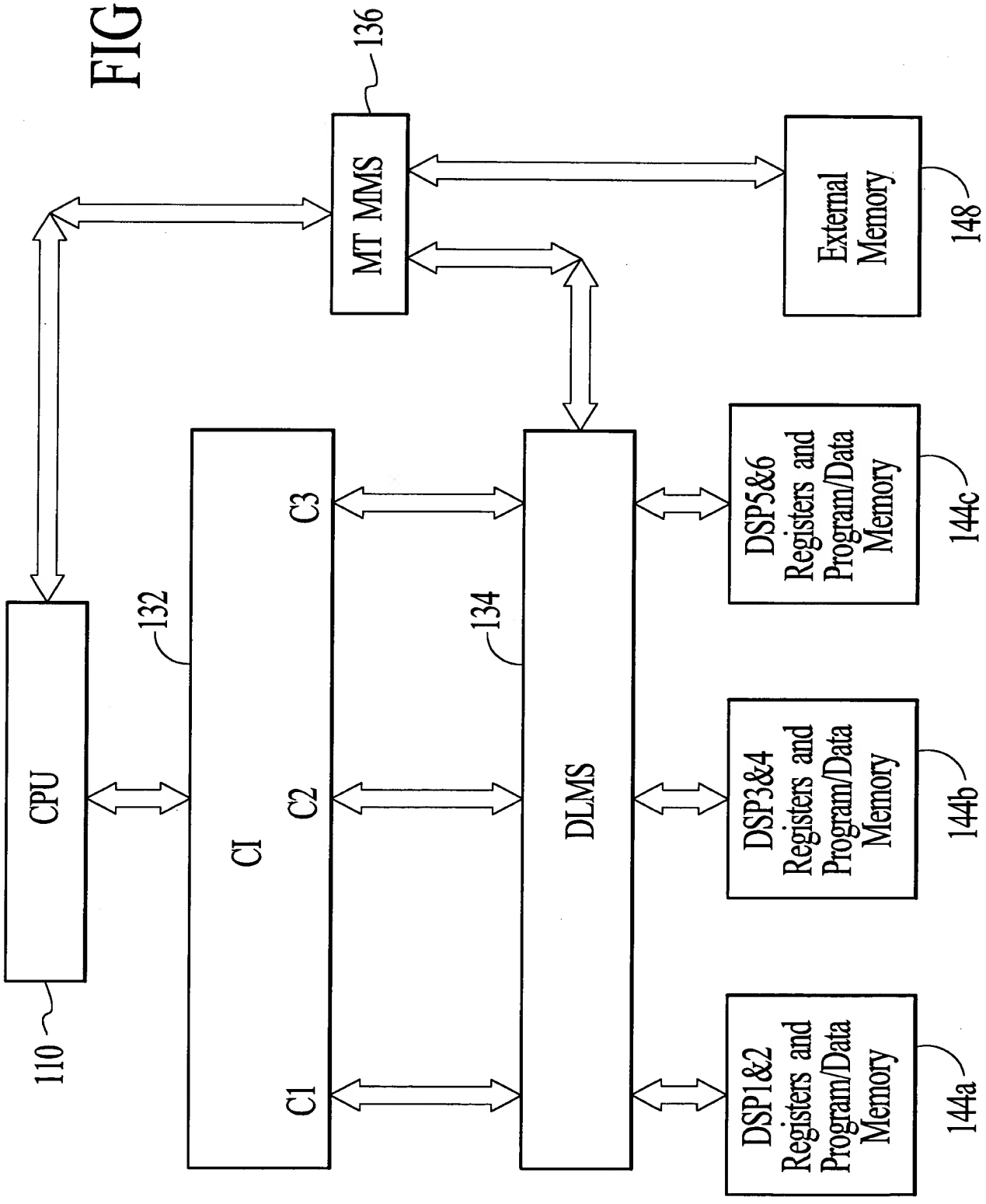

CPU
110
122
CI
C1
C2
C3
DSP1&2
DSP3&4
DSP5&6
124a
124b
124c

FIG. 8B

FIG. 9A


110
CPU
132
CI
C1
C2
C3
134
DLMS
136
MT MMS
148
External Memory
144a
DSP1&2 Registers and Program/Data Memory
144b
DSP3&4 Registers and Program/Data Memory
144c
DSP5&6 Registers and Program/Data Memory

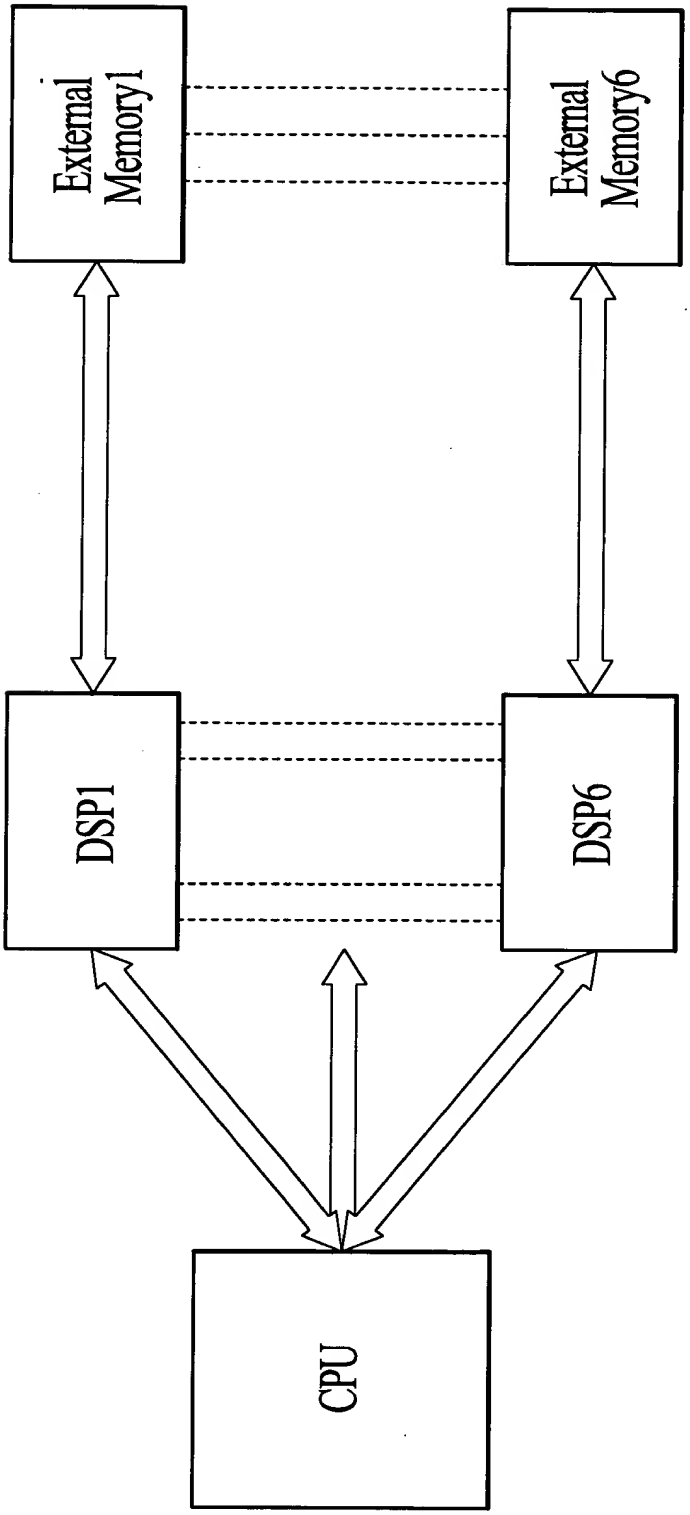


FIG. 9B

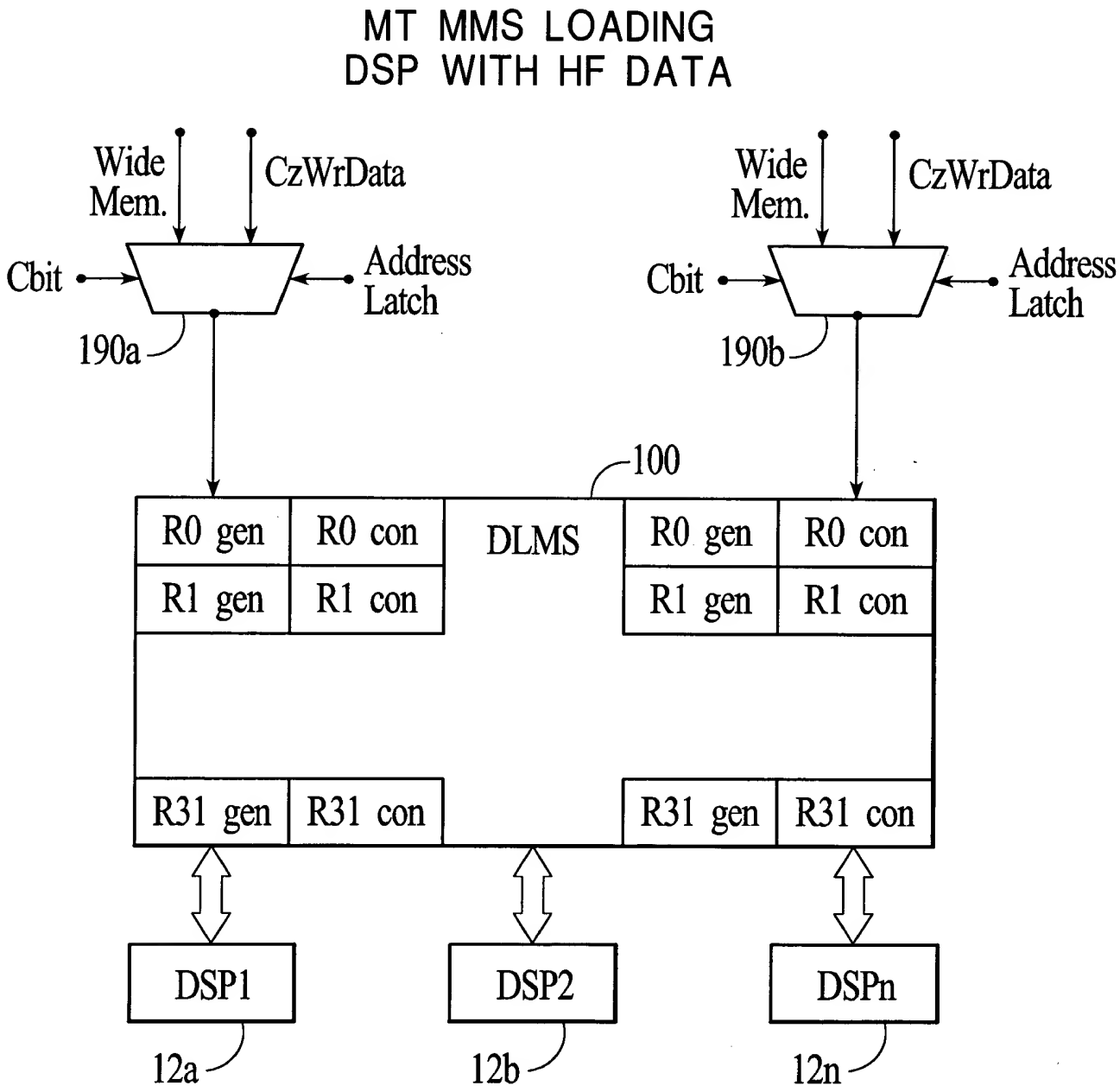

MT MMS LOADING
DSP WITH HF DATA
Wide Mem.
CzWrData
Cbit
Address Latch
190a
Wide Mem.
CzWrData
Cbit
Address Latch
190b
100
R0 gen
R0 con
R1 gen
R1 con
DLMS
R0 gen
R0 con
R1 gen
R1 con
R31 gen
R31 con
R31 gen
R31 con
DSP1
DSP2
DSPn
12a
12b
12n

FIG. 10

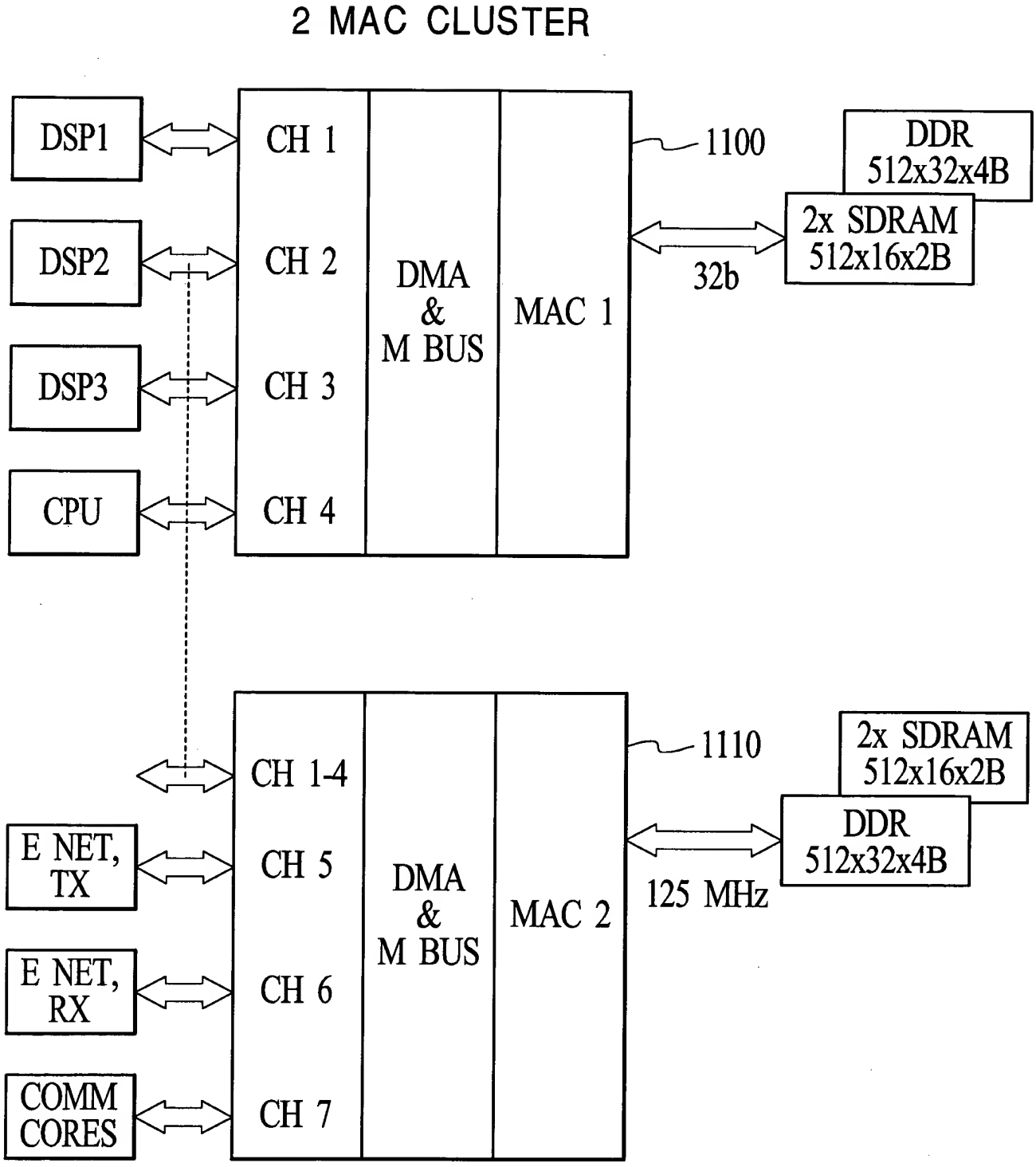

2 MAC CLUSTER
DSP1
DSP2
DSP3
CPU
CH 1
CH 2
CH 3
CH 4
DMA & M BUS
MAC 1
1100
DDR 512x32x4B
2x SDRAM 512x16x2B
32b
CH 1-4
E NET, TX
E NET, RX
COMM CORES
CH 5
CH 6
CH 7
DMA & M BUS
MAC 2
1110
2x SDRAM 512x16x2B
DDR 512x32x4B
125 MHz

FIG. 11

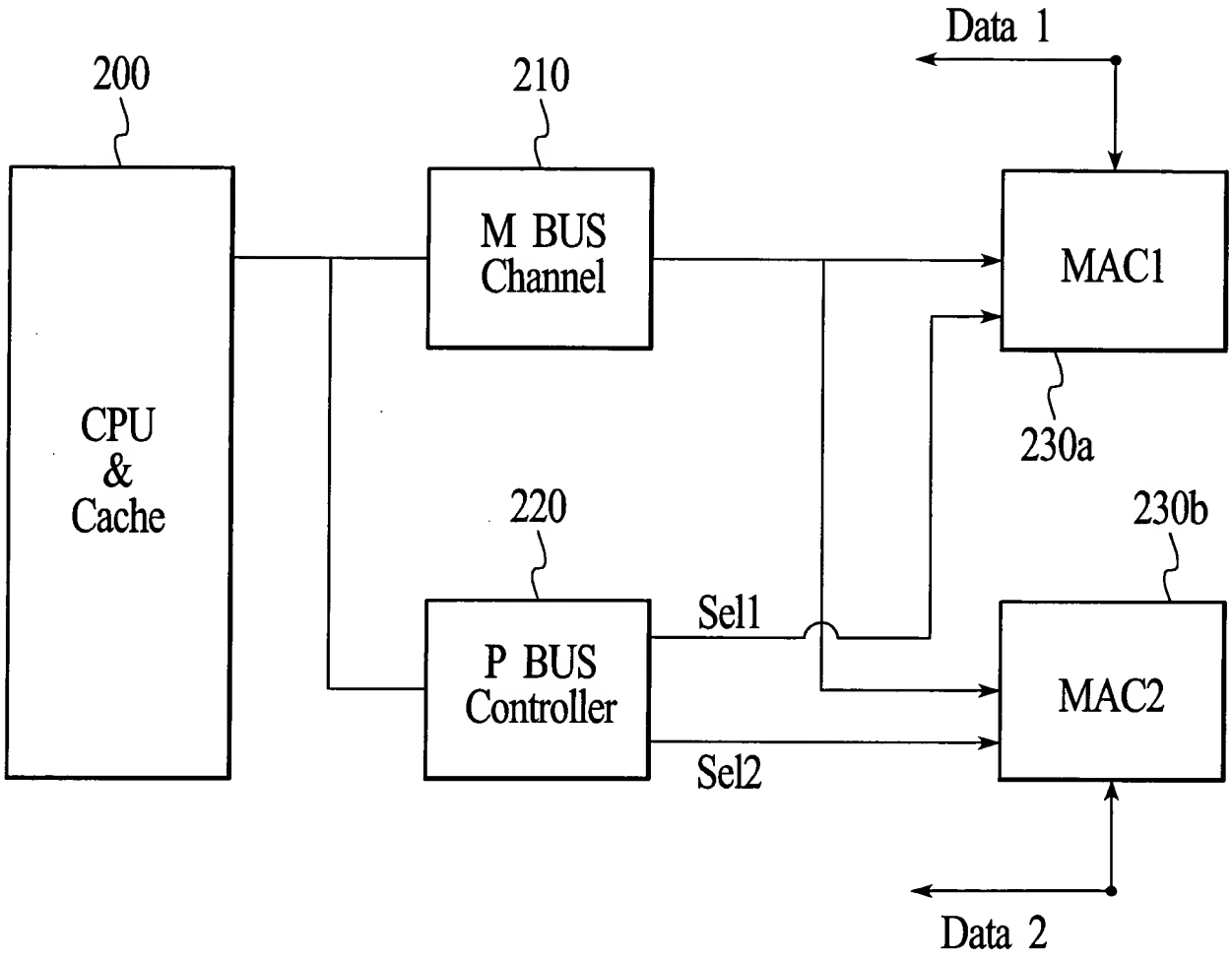

Data 1
200
210
M BUS
Channel
MAC1
CPU
&
Cache
230a
220
230b
Sel1
P BUS
Controller
MAC2
Sel2
Data 2

FIG. 12

DMA & MAC CLUSTER

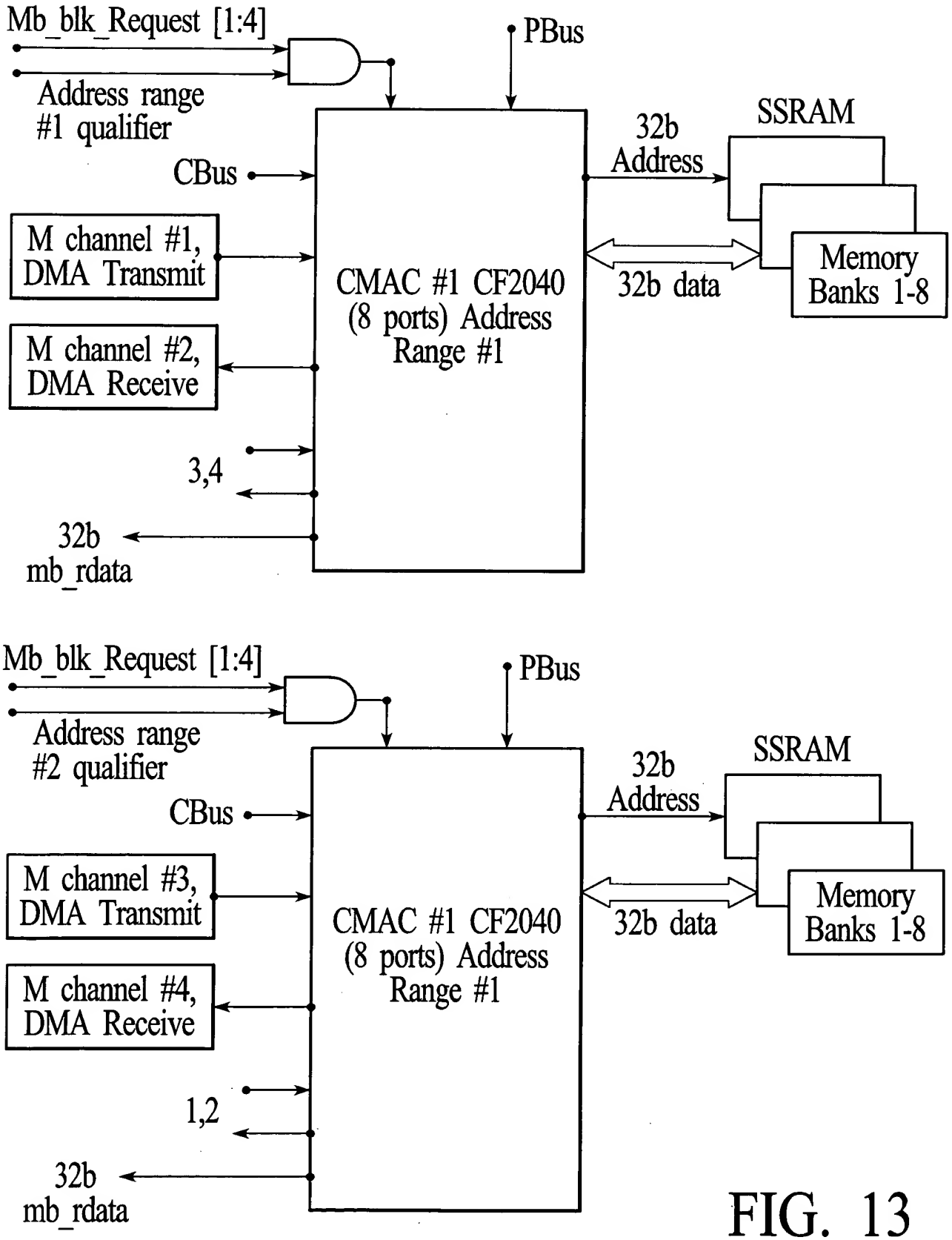


FIG. 13

MULTIPLEXING THE DATA BUS
TO INDIVIDUAL CHANNELS

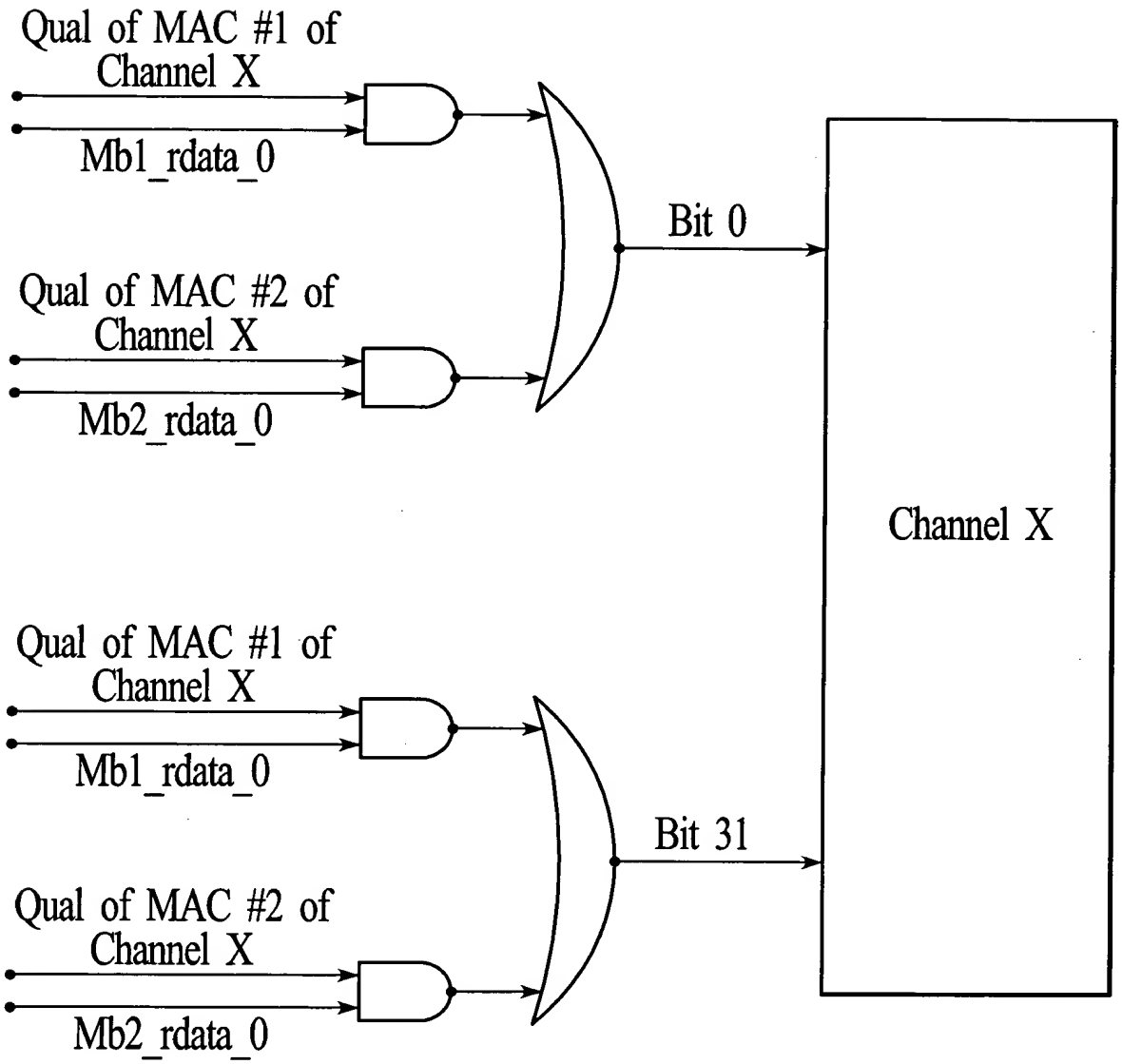
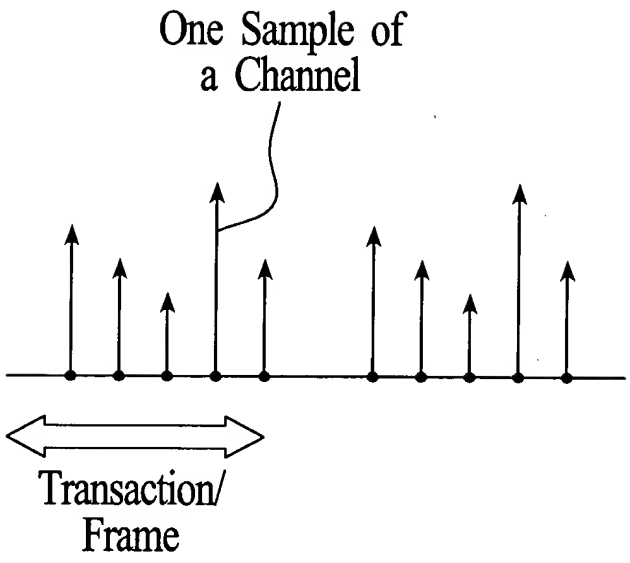


FIG. 14

REAL TIME LOAD MANAGEMENT



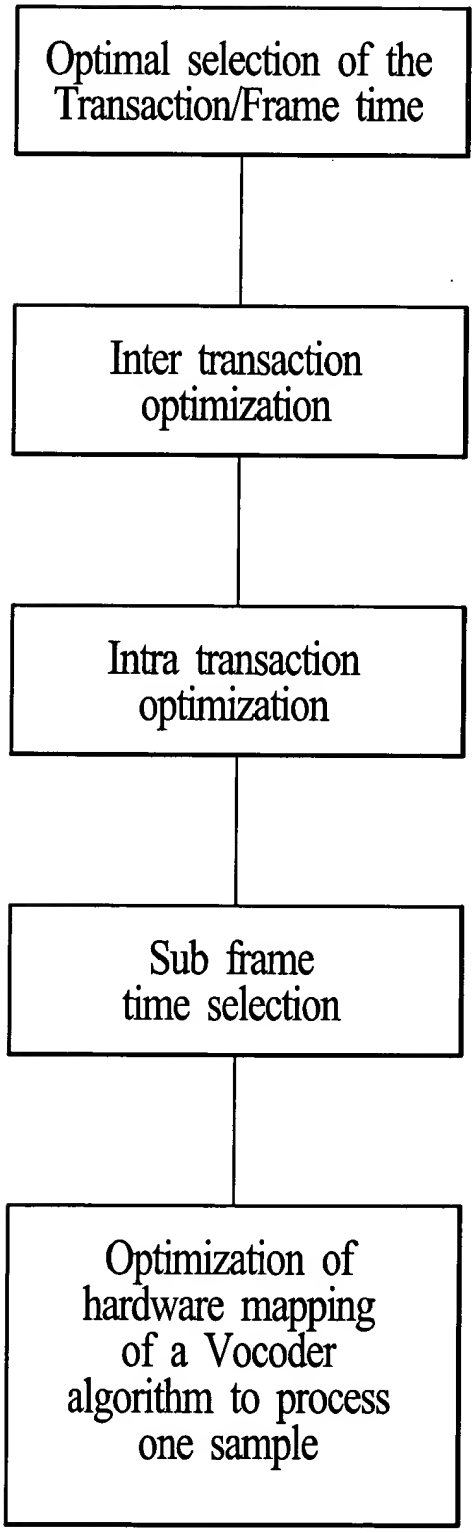


FIG. 15

DLMS PARALLEL WORD TRANSFER

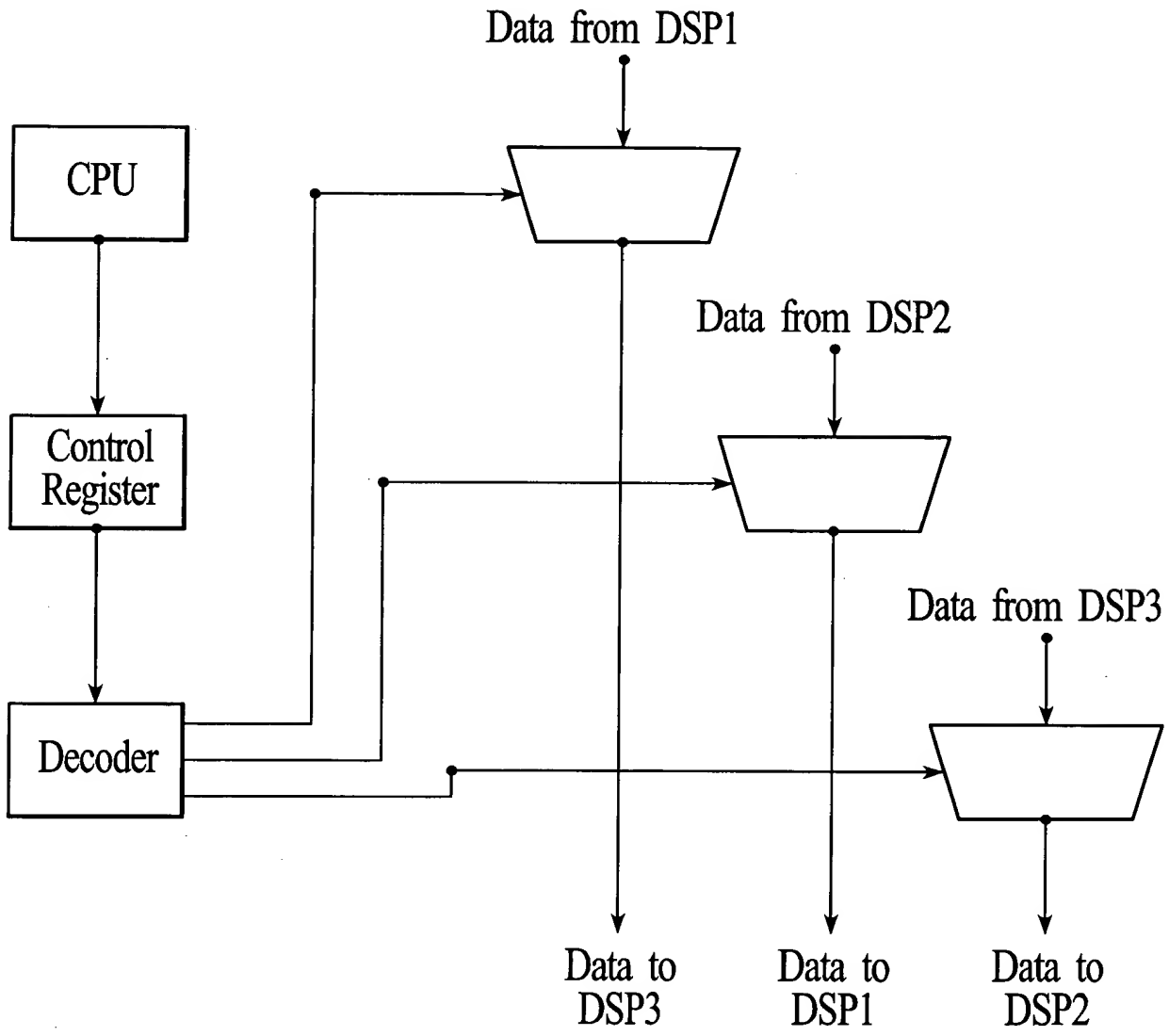


FIG. 16

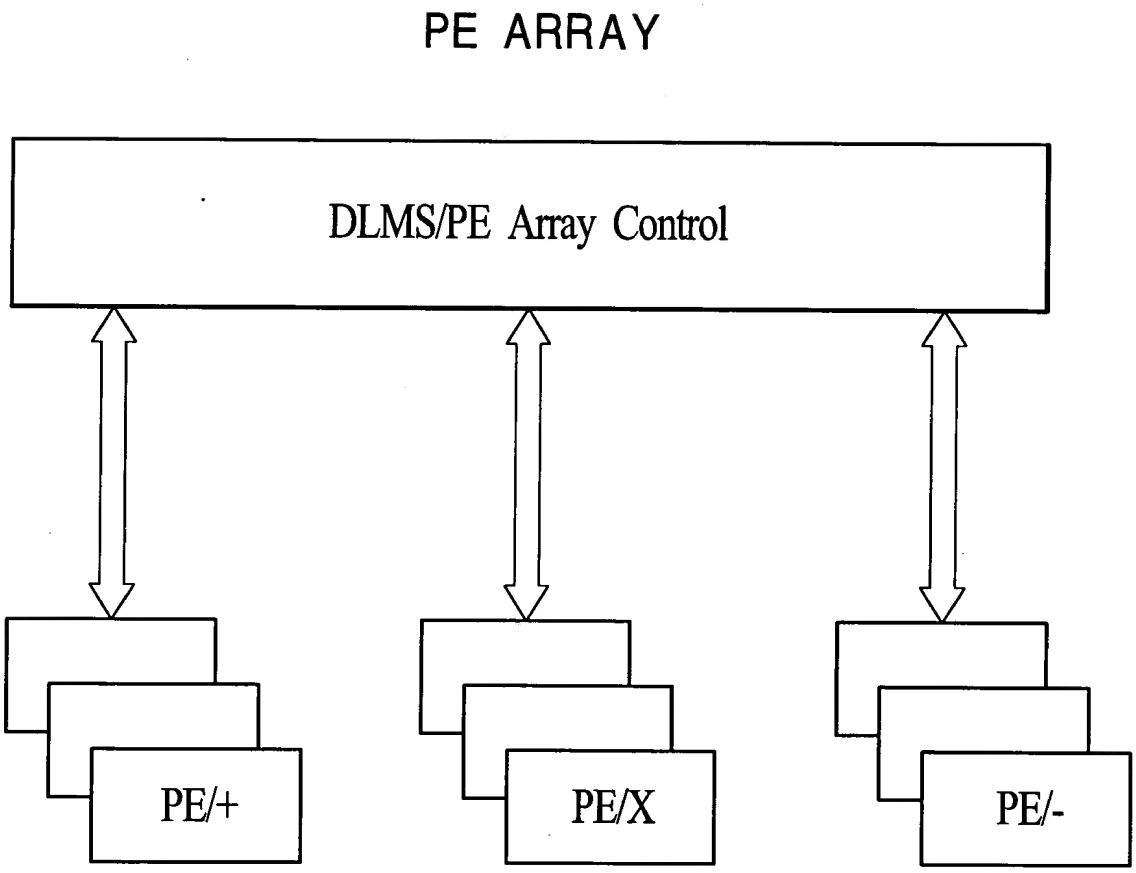


FIG. 17

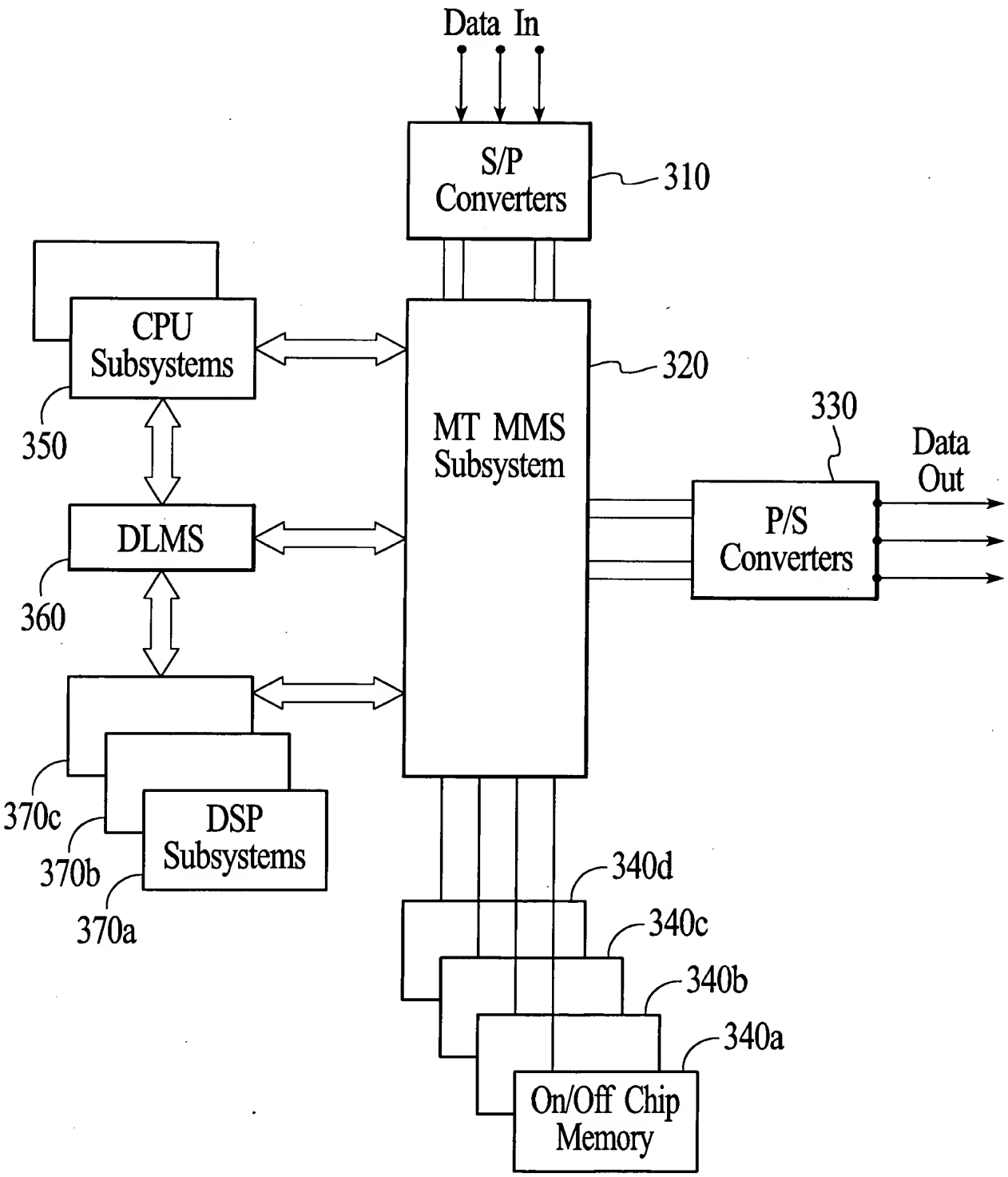

Data In
S/P Converters
310
CPU Subsystems
350
DLMS
360
DSP Subsystems
370c
370b
370a
MT MMS Subsystem
320
330
P/S Converters
Data Out
340d
340c
340b
340a
On/Off Chip Memory

FIG. 18A

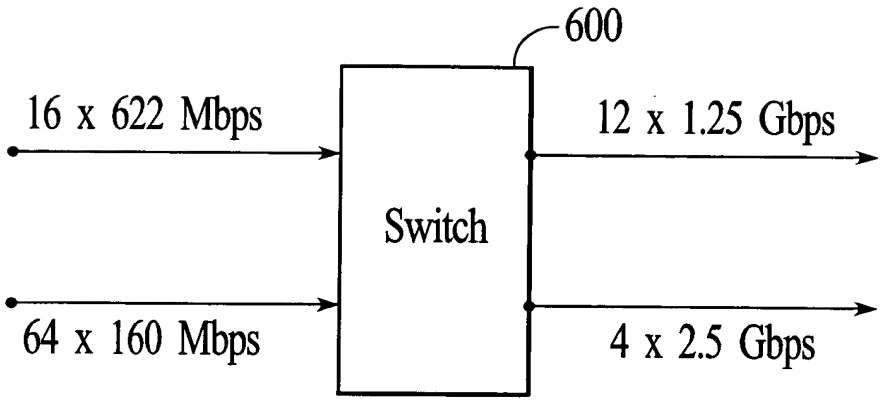


FIG. 18B

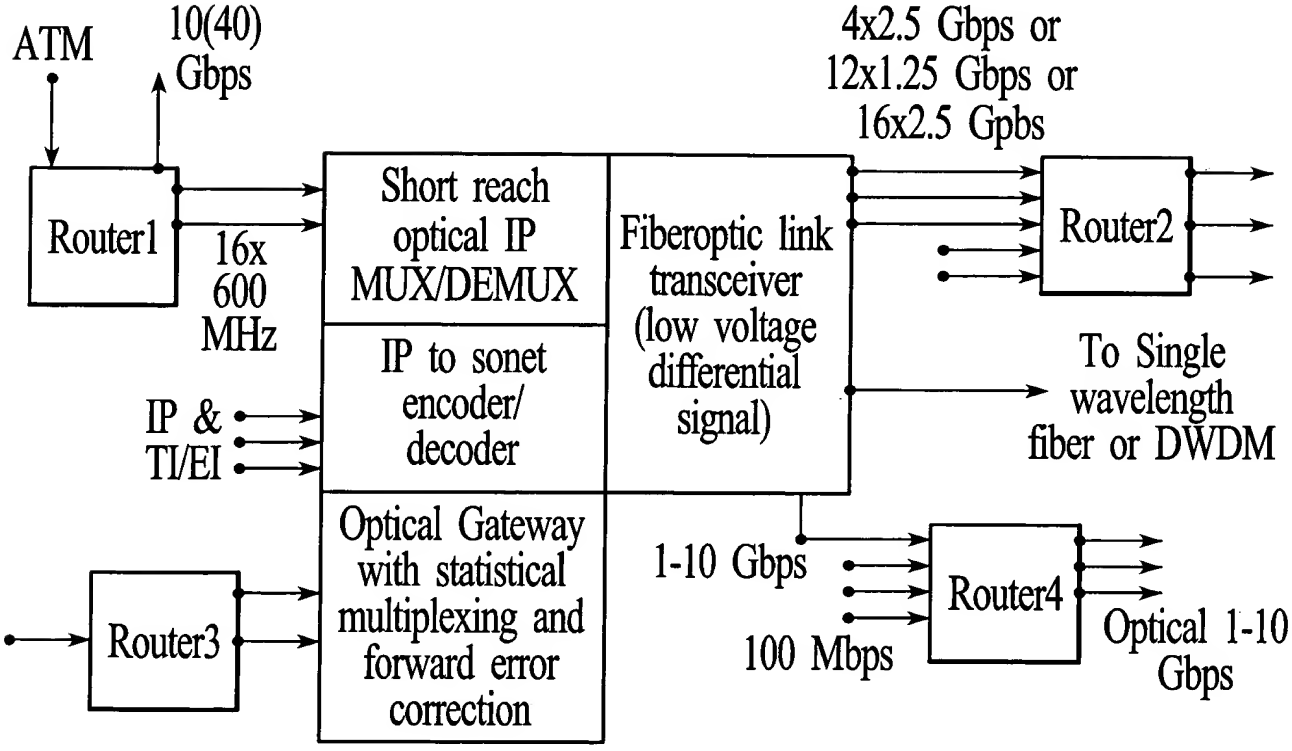


FIG. 18C